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XIOMARA D. JUNCO

Docket No.: GR 97 P 1903

Date: January 14, 2000

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Enclosed herewith are the necessary papers for filing the following application for Letters Patent:

Applicant : HANSJÖRG REICHERT ET AL.

Title : METHOD AND APPARATUS FOR PRODUCING A CHIP-SUBSTRATE CONNECTION

1 sheet of formal drawings in triplicate.
A check in the amount of $690.00 covering the filing fee.
Information Disclosure Statement and 13 References.
PCT Publication (cover sheet only).

This application is being filed without a signed oath or declaration under the provisions of 37 CFR 1.53(d). Applicants await notification of the date by which the oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted,

For Applicants

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LAG:tg

GR 97 P 1903

METHOD AND APPARATUS FOR PRODUCING A CHIP-SUBSTRATE CONNECTION

Cross-Reference to Related Application:

This is a continuation of copending International Application PCT/DE98/01737, filed June 24, 1998, which designated the United States.

Background of the Invention:

Field of the Invention:

The invention relates to a method and an apparatus for producing a chip-substrate connection by alloying or brazing, using a solder with a two metal-containing constituents X and Y, the first constituent X containing in particular gold or a similar precious metal. The invention furthermore relates to a solder for the production of a chip-substrate connection, and to a semiconductor component with a semiconductor chip which is secured to a substrate by alloying or brazing.

When a rear side of a semiconductor chip is joined to a substrate, which is usually referred to as chip or die bonding, the requirements with regard to sufficient mechanical fixing and also good thermal and electrical conductivity must be fulfilled individually or jointly, depending on the application. An important factor is the compatibility of the

chip and the substrate, that is to say the matching of the two participants in the joint in terms of their expansion behavior under thermal loading. At the present time, essentially three distinguishable methods of chip securing are customary: alloying (brazing), soldering (soft soldering), and bonding. The preferred area of application according to the present invention is alloying or brazing; in a known bonding method in the AuSi system, a eutectic joint between the semiconductor chip and the substrate is produced at the lowest melting temperature of the participants in the joint. Alloy formation takes place at a temperature that lies well below the melting temperature of the individual components Au and Si. This temperature is not high enough to damage the semiconductor structure and therefore the electrical function. During the alloying operation, the chip and the substrate are heated to this temperature, with a slight pressure being applied and with the chip being rubbed on in a circular movement in order to improve the contact. When the melting point in accordance with the liquidus-solidus curve of the phase diagram is reached, the solder becomes liquid, and the bonding process commences. For reasons of cost, the heating operation generally takes place very quickly, and does not go beyond thermodynamic equilibrium states. In contrast, the cooling operation takes place significantly more slowly. First, the component that is present in excess crystallizes out, until, at the solidification point, the eutectic mixing ratio is

reached once again. During solidification of the eutectic molten material, the two components crystallize separately, so that the microstructure of the solidified eutectic reveals uniformly distributed Si and Au crystals.

The likelihood of the chip breaking is minimized by providing a chip-substrate connection which is as uniform as possible over a large surface area and by low internal stresses. The quality of the joint is controlled by the flow properties of the solder, and the internal stress is controlled by the temperature difference between solder solidification and temperature of use.

Summary of the Invention:

It is accordingly an object of the invention to provide a method and an apparatus for producing a chip-substrate connection which overcome the above-mentioned disadvantages of the prior art methods and devices of this general type, in which the risk of a chip breaking is as low as possible.

With the foregoing and other objects in view there is provided, in accordance with the invention, a method for producing a chip-substrate connection, which includes performing one of alloying and brazing a chip to a substrate using a solder containing at least two components with at least two metal-containing constituents including a first

constituent X containing a precious metal and a second constituent Y being consumed in a soldering operation by one of reacting and being dissolved by materials being joined, and the solder having a hypereutectic concentration of the second constituent Y.

According to the invention, the solder has a hypereutectic concentration of the second constituent Y. In this case, the constituent Y constitutes that component of the solder containing two or more components which is consumed during the soldering operation by reacting or being dissolved in the layers which are to be joined. The same applies, mutatis mutandis, to multi-component systems.

A particularly preferred, low-melting solder is in this case an AuSn solder with a hypereutectic concentration of tin. The AuSn solder preferably contains more than 20% by weight Sn.

The invention offers in particular the below listed advantages.

Compared to the known eutectic AuSi or eutectic AuGe solders which are vapor-deposited on the rear side of the wafer, the use of an AuSn solder with a hypereutectic Sn concentration provides chip-alloying temperatures which are up to 100° Celsius lower, and therefore considerably reduced thermal

stresses, and consequently a lower risk of the chip breaking. Furthermore, the invention allows improved homogeneity and wetting of the solder layer.

Compared to a eutectic AuSn solder, the invention has the advantage above all of a lower alloying temperature. During the coating and mounting process, the Sn content of the eutectic AuSn falls, since both the required barrier between AuSn and Si and the lead frame surface (for example containing Ag) absorb Sn during mounting. Consequently, the melting temperature of the AuSn solder rises. Particularly in the case of sputtered eutectic AuSn, the alloying temperature that is required for joining is almost as high as that of an AuSi alloy.

Compared to epoxy adhesives, the invention provides the advantage of improved thermal conductivity of the joint, improved homogeneity of the joint, and above all saving on the adhesive and bonding process during mounting.

Compared to soldering with a preform, the method according to the invention provides above all a reduction in costs during mounting.

Preferably, the solder is deposited on the rear side of the chip, in particular by sputtering. Naturally, this takes

place in the wafer composite of the semiconductor chips, so that the term chip also encompasses the chip that is still in the wafer composite.

It is particularly advantageous for the deposition to have a composition by weight of the constituents X to Y of 70 to 30, i.e. preferably a composition of AuSn = 70/30. The layer of solder is sputtered onto the rear side of the wafer with a thickness of from about 1 µm to about 2 µm, preferably of about 1.5 µm.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a method and an apparatus for producing a chip-substrate connection, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description

of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 is a phase diagram of AuSn;

Fig. 2A is a fragmented, perspective view of a semiconductor chip which has been alloyed on a lead frame using a hypereutectic AuSn solder according to the invention; and

Fig. 2B a diagrammatic, enlarged, sectional view of detail X from Fig. 2A.

Description of the Preferred Embodiments:

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown that for an AuSn composition the eutectic temperature is 278° Celsius, and a specific composition contains 20% Sn and 80% Au (percent by weight). Therefore, alloy formation takes place at a temperature that lies well below the melting temperature of the individual components. In accordance with the fundamental concept of the invention, an AuSn solder with a hypereutectic concentration of tin is used, so that the AuSn solder contains more than 20% by weight

Sn. The result is a sufficiently low viscosity of the solder at temperatures of below 380° Celsius for mounting in surface mounting devices or SOT housings, since diffusion of Sn into adjoining layers of metal causes the composition of the AuSn to move away from the tin-rich phase toward the eutectic point, so that a gold-rich solder phase which lies above the eutectic is avoided. The melting temperature of the AuSn mixture rises very steeply if Au is in excess, while the increase in the melting point is significantly less if the mixture is enriched with Sn. A loss of Sn from an Sn-rich solder according to the invention results in a continuous reduction in the melting point during the soldering operation, thus promoting the soldering operation. The melting temperature is reduced locally in particular at the contact point between solder and a lead frame (for example Ag), where the Sn depletion takes place, thus improving the flow properties of the solder. For this reason, an excess supply of Sn results in reproducible mounting conditions at low temperatures. This effect is greatly emphasized in particular in the case of thin layers of solder, as are conventionally used when coating the rear side of wafers.

Figs. 2A and 2B show a connection between a semiconductor chip 1 on a central "island" 2 of a metallic lead frame 3, which is produced by alloying or brazing. The prefabricated metallic lead frames 3 represent a very widespread form of substrate,

in particular for use in plastic housings. The enlarged partial view shown in Fig. 2B shows the sequence of layers in more detail. A rear side of the semiconductor chip 1 is provided with an adhesion or diffusion barrier 4, which preferably contains Ti/Pt. Reference numeral 5 denotes a layer of solder that has been sputtered onto the rear side of the wafer with a thickness of typically 1.5 µm. To allow the chip-substrate connection to have a sufficiently low resistance, it may be necessary for a doping layer, for example of AuAs, or a contact implantation 6 also to have been incorporated beforehand.

We claim:

1. A method for producing a chip-substrate connection, which comprises:

performing one of alloying and brazing a chip to a substrate using a solder containing at least two components with at least two metal-containing constituents including a first constituent X containing a precious metal and a second constituent Y being consumed in a soldering operation by one of reacting and being dissolved by materials being joined, and the solder having a hypereutectic concentration of the second constituent Y.

2. The method according to claim 1, which comprises providing the second constituent Y of the solder with tin having the hypereutectic concentration.

3. The method according to claim 1, which comprises using a gold-tin compound (AuSn) as the solder with a hypereutectic Sn concentration.

4. The method according to claim 3, which comprise providing the gold-tin compound a tin concentration being greater than 20% by weight.

5. The method according to claim 1, which comprises depositing the solder on a rear side of the chip.

6. The method according to claim 5, which comprises providing the solder with a composition by weight of the first constituent X to the second constituent Y of 70 to 30.

7. The method according to claim 5, which comprises applying the solder with a thickness of from about 1 µm to about 2 µm to the rear side of the chip.

8. The method according to claim 1, which comprises using gold as the precious metal.

9. The method according to claim 1, which comprises depositing the solder on a rear side of the chip by sputtering.

10. The method according to claim 5, which comprises applying the solder by sputtering with a thickness of about 1.5 µm to the rear side of the chip.

11. A solder for use in producing a chip-substrate connection, comprising:

a solder composition containing at least two components with at least two metal-containing constituents including a first constituent X formed of a precious metal and a second constituent Y being consumed during a soldering operation by one of reacting and being dissolved by materials which are to be joined, and said solder composition has a hypereutectic concentration of said second constituent Y.

12. The solder according to claim 11, wherein said second constituent Y contains tin with a hypereutectic concentration.

13. The solder according to claim 11, wherein said precious metal is gold.

14. The solder according to claim 11, wherein said solder composition has a composition by weight of said first constituent X to said second constituent Y of 70 to 30.

15. A semiconductor component, comprising:

a solder containing at least two components with at least two metal-containing constituents including a first constituent X being formed of a precious metal and a second constituent Y being consumed during a soldering operation by one of reacting and being dissolved in materials which are to be joined, and

said solder having a hypereutectic concentration of said second constituent Y;

a substrate; and

a semiconductor chip secured to said substrate by one of alloying and brazing using said solder.

16. The semiconductor component according to claim 15, wherein said solder contains a gold-tin compound (AuSn) with a hypereutectic Sn concentration.

Abstract of the Disclosure:

A method and an apparatus for producing a chip-substrate connection by alloying or brazing, using a solder containing two or more components with at least two metal-containing constituents X and Y. The first constituent X contains in particular gold or a similar precious metal, and the second constituent Y being consumed in the soldering operation by reacting or being dissolved in the materials or layers which are to be joined. The solder has a hypereutectic concentration of the second constituent Y. The invention furthermore relates to a solder for the production of a chip-substrate connection, and to a semiconductor component with a semiconductor chip which is secured to a substrate by alloying or brazing.

REL/tg

Fig 1

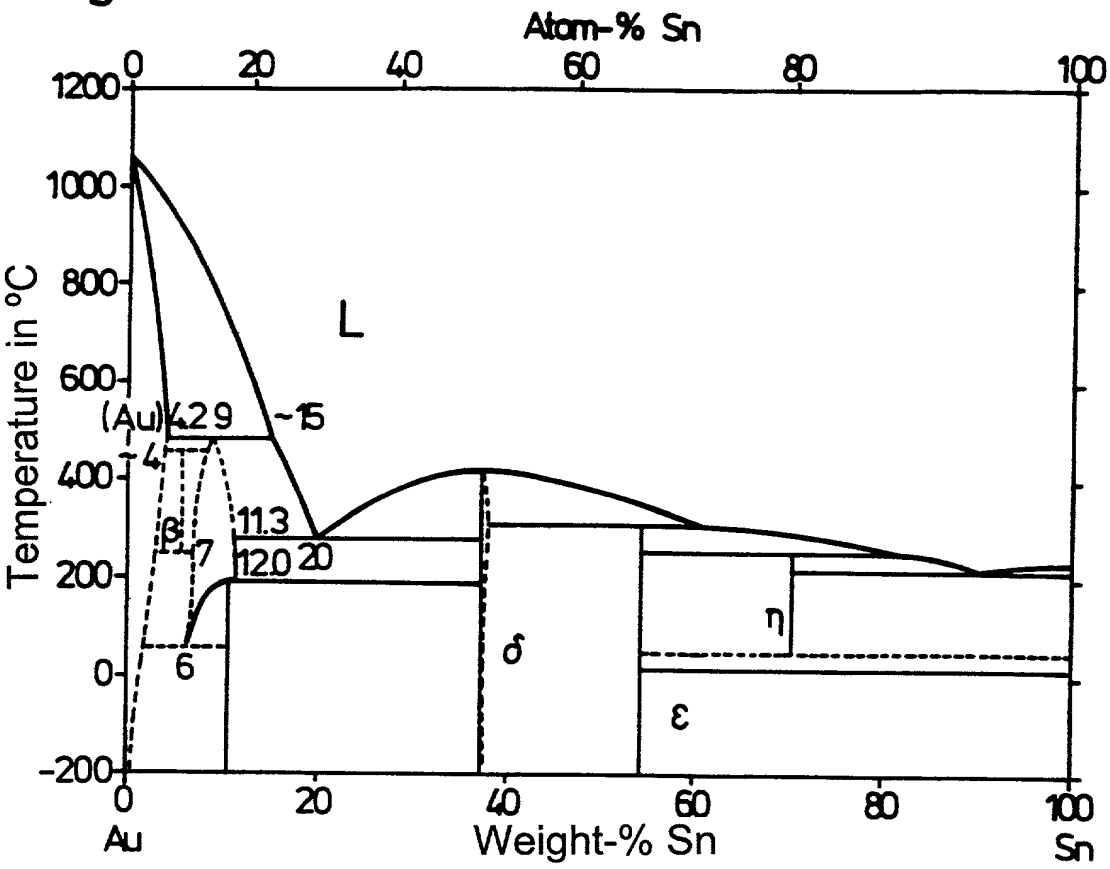


Fig 2A

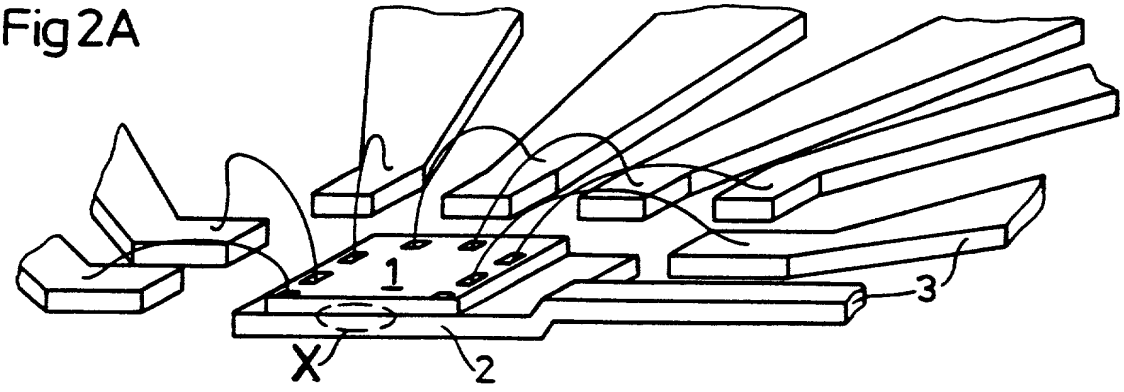
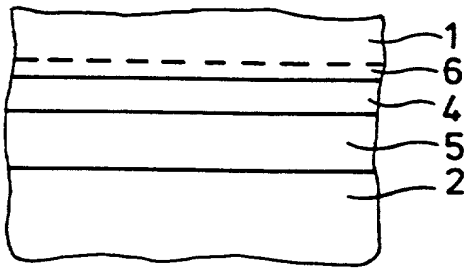


Fig 2B

X:



Docket No.: GR 97 P 1903

COMBINED DECLARATION AND POWER OF ATTORNEY
IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND APPARATUS FOR PRODUCING A CHIP-SUBSTRATE CONNECTION

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

German Application No. 197 30 118.5, filed July 14, 1997, the International Priority of which is claimed under 35 U.S.C. §119; and International Application No. PCT/DE98/01737, filed June 24, 1998, the Priority of which is claimed under 35 U.S.C. §120.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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